AN1628/D

Understanding Power Transistors Breakdown Parameters

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APPLICATION NOTE

INTRODUCTION

Among the electrical parameters of a Bipolar power transistor, the breakdown related ones are the most critical to measure. As a matter of fact, as the breakdown voltage can be pretty high, the instantaneous power dissipated during the test must be accurately controlled to avoid a local hot spot on the chip. On the other hand, the breakdown mechanisms are prone to high frequency oscillations and care must be observed to accurately measure this parameter. This application note gives a definition of the breakdown parameters and the associated physics of semiconductor devices. A chapter describes the test techniques and methods recommended to perform this kind of measures.

Since most of the high voltage bipolar transistors are NPN type, all the analysis carried out in this note will be referenced to NPN devices. The PNP mechanisms are essentially the same, with reverse polarities of all biases.

BREAKDOWN MECHANISM

Let us first consider the Collector to Base junction. Like a $p-n$ diode, the avalanche process limits the collector−base voltage the transistor can sustain. When the voltage is large enough, the n−side depletion region will reach the n+ contact diffusion and, if the voltage increases further, the contact will supply electron to the $p-n$ junction. At this point, the Collector−Base junction is essentially shorted and the current is limited by the external resistances.

Basically, three mechanisms control the breakdown: thermal instability, tunneling effect and avalanche multiplication.

THERMAL INSTABILITY

The breakdown for thermal instability is the result of large increase of leakage current when the junction temperature increases. Germanium based devices are more sensitive to this mechanism compare to the Silicon. The process snowball as the leakage current increases, yielding higher junction temperature which can lead to the destruction of the chip if it extends above the melting point of the semiconductor material.

TUNNELING EFFECT

When the electrical field approaches 10^6 V/cm in Silicon, a significant current begins to flow by means of the band to band tunneling process. To get such a high field, the junction must have relatively high doping concentration on both side of the p−n junction. As a matter of fact, the field may be so high that it creates enough force on a covalently bounded electron to free it. This creates two carriers, a hole and an electron to contribute to the current. From an energy−band point of view, in this breakdown process an electron makes a transition from the valence band to the conduction band without the interaction of any other particles.

The breakdown mechanism for silicon device with breakdown voltage lower than 4Eg/q comes from the tunneling effect. For junctions having breakdown voltage in excess of 6Eg/q, the mechanism is generated by avalanche multiplication. At voltages between 4Eg/q and 6Eg/q, the breakdown is a combination of the two effects.

Since the energy band gap in silicon decreases with temperature, the breakdown voltage due to tunneling effect in these semiconductors has a negative temperature coefficient. This temperature effect can be used to differentiate the tunneling effect from the avalanche mechanism which has a positive temperature coefficient.

One must point out that the tunneling effect is dominant for zener voltage in the 5 V to 6 V range. This mechanism is not present for high voltage junctions since the doping concentration is too low to generate the tunneling effect.

AVALANCHE MULTIPLICATION

This mechanism, also named impact ionization, is the most important one in junction breakdown since the avalanche breakdown voltage imposes an upper limit on the reverse bias of the collector voltage. The value at which breakdown occurs depends on the structure of the junction and the dopant concentration used to manufacture the transistor. Both the structure and the epitaxy being controlled, the breakdown voltage of a given semiconductor is reasonably predictable at the design stage.

In this process, free carriers can gain enough energy from the field between collisions to break covalent bonds in the lattice when they collide with it. Consequently, every carrier interacting with the lattice creates two additional carriers and the mechanism snowballs as three carriers can also participate to the collisions. This leads to a sudden multiplication of carriers in the space−charge region when the electrical field becomes large enough to trigger the avalanche.

Let us consider an electron traveling in the space−charge region of a reverse biased pn junction. The electron travels, on average, a distance L (the mean free path) before losing energy by interacting with an atom in the lattice. The energy ΔE gained from the field *E* by the moving electron between collisions is:

$$\Delta E = q \int_0^L E.\,dx \qquad (1)$$

Assuming the electron has accumulated enough energy from the field prior colliding with an atom, the bond between the atom core and one of the bound electron can be broken during the collision. This creates three resulting carriers which are free to leave the region of the collision. A simplified schematic representation is given in Figure 1.

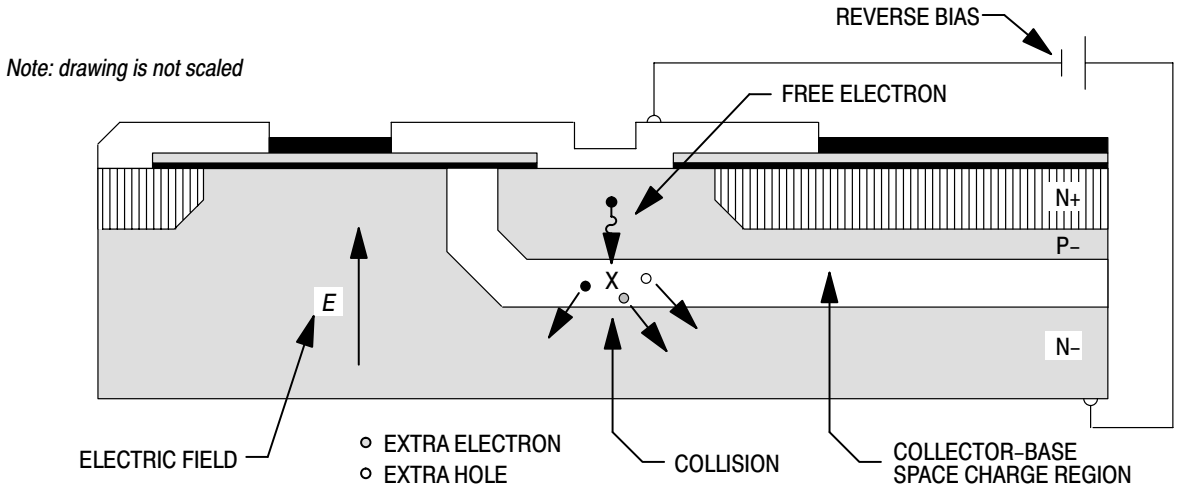
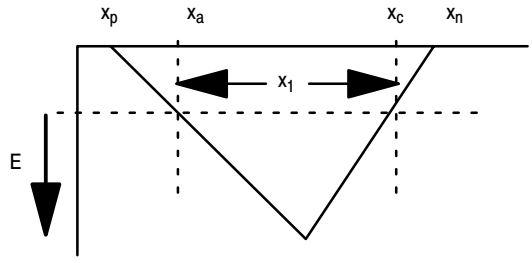
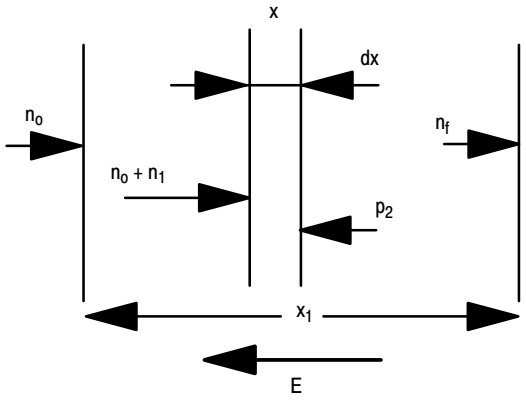


Figure 1. Simplified Representation of the Avalanche Process in a Junction

Near the edge of the space charge region, the electric field is low and practically no carriers can gain enough energy from the field to create a hole−electron pair before they lose their kinetic energy in a collision with the lattice. Consequently, the avalanche is confined to the central area of the space charge region where the field is sizable. This is represented in Figure 2, the central region being identified by x_1.



(a) Ionization occurs in the high field area x_1 of the space charge region



(b) Carriers pair are created in the region dx at x, by electrons flowing from the left and hole flowing from the right

Figure 2. Ionization Process Location for a Non Punch Trough Structure

Let us consider the number of carriers created by avalanche in a small volume of width dx located within x_1 at x (see Figure 2b). Let n_o = density of electrons entering x_1 from the left at x_a.The avalanche phenomenon will increase this density between x_a and x_c in a way that the electrons entering the volume Adx at x from the left have a density $n_o + n_1$. The probability that electrons create electron−hole pairs when travelling through dx is given by the product of the ionization coefficient α**n**, times the length dx. Since the electrons gain energy more rapidly when the field is higher, the ionization coefficient is a function of the electric field, hence of the position in the semiconductor.

In the same manner, the density of holes will increase as a consequence of the avalanche, and the $\alpha_{\mathbf{p}}$ factor represent the ionization coefficient for the holes.

Let n_f be the density of electrons that reaches x_c:

$$n_f = n_o + n_1 + n_2 \tag{2}$$

where n_2: density of electrons created between x and x_c.

Since electrons and holes are created in pair, $n_2 = p_2$, we may write:

$$\frac{dn}{dx} = (\alpha_n - \alpha_p)(n_o + n_1) + \alpha_p n_f \tag{3}$$

Assuming that $\alpha = \alpha_n = \alpha_p$, we can rewrite equation 3 as follows:

$$n_f - n_o = n_f \int_{xa}^{xc} \alpha \, dx \tag{4}$$

The ratio of the density of electrons n_f leaving the space−charge region to the density n_o entering is called the multiplication factor **M**:

$$\mathbf{M} = \frac{n_f}{n_o} = \frac{1}{1 - \int_{xa}^{xc} \alpha \, dx} \tag{5}$$

As the integral in the denominator of equation 5 approaches unity, the **M** factor increases to infinity. Therefore, the avalanche will occur when:

$$\int_{xa}^{xc} \alpha \, dx = 1 \tag{6}$$

The density of ionizing collisions at x is proportional to **n*** which represent the density of excited electrons arriving at x with enough energy to create the electron−hole pair. The density **n***, in turn, is the total electron density **n** times the probability that an electron has not collided in a distance **d** necessary to get the right energy:

$$\mathbf{n^*} = \mathbf{n} \exp\left(-\frac{\mathbf{d}}{L}\right) \tag{7}$$

The length **d** may be derived from equation 1 by letting E_1 being the minimum energy necessary to create the ionization process, and *E* being the average field that accelerates the electron:

$$d = \frac{E1}{qE} \tag{8}$$

Since the ionization coefficient depends strongly on the electric field, the multiplication factor also increases rapidly with field. Consequently, a small increase in field, as the voltage approaches breakdown, causes a sharp increase in current as observed on a curve tracer. Not only does the ionization coefficient vary with field, hence with the position, in the space charge region, but the width of the space charge region varies also with voltage. Therefore, the evaluation of **M** with equation 5 is difficult and a good approximation can be derived from the simplified equation 9:

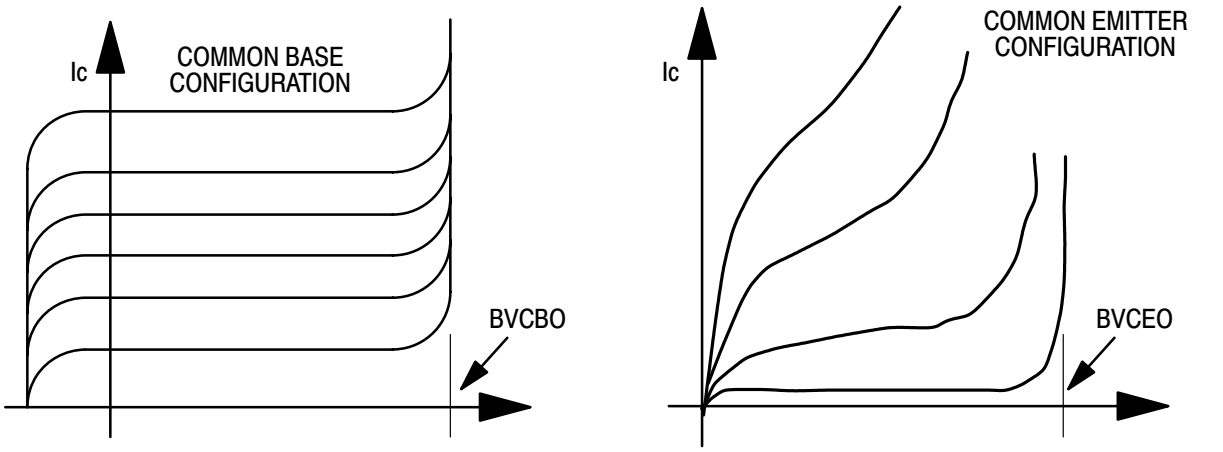
$$\mathbf{M} = \frac{1}{1 - \left(\frac{Vr}{Bv}\right)^n} \tag{9}$$

with $2 < n < 6$

Vr: the reverse voltage applied across the junction

Bv: the breakdown voltage.

In the common Base configuration, the breakdown due to the impact ionization (avalanching) gives a well defined voltage as depicted in Figure 3a, the effect of the current coming from the emitter having little effect on the breakdown.



(a) Under breakdown, the emitter current is not affected

(b) At low impact ionization rate, the base current starts to increase, yielding an emitter current increase and, eventually, a collector current runaway

Figure 3. Common Base and Common Emitter Breakdown Typical Curves

For the common Emitter configuration, the breakdown is not as sharply reflected in the transistor output characteristics as depicted in Figure 3b, and occurs at a lower voltage BVCEO. In this configuration, as soon as the impact ionization process starts, the secondary holes are injected into the base, yielding a base current which, in turns, leads to an increase in the emitter current and a current runaway may eventually occurs as the mechanism snowballs.

SECOND BREAKDOWN

The use of power transistor is limited by the second breakdown phenomenon which is an abrupt decrease of the device voltage capability with a simultaneous internal constriction of current. Figure 4 shows a typical Ic/Vc characteristic of a transistor under second breakdown. The avalanche breakdown (also named first breakdown) occurs when the voltage applied across the junction reaches the value specific for this device as discussed above. As the voltage is increased, the second avalanche occurs.

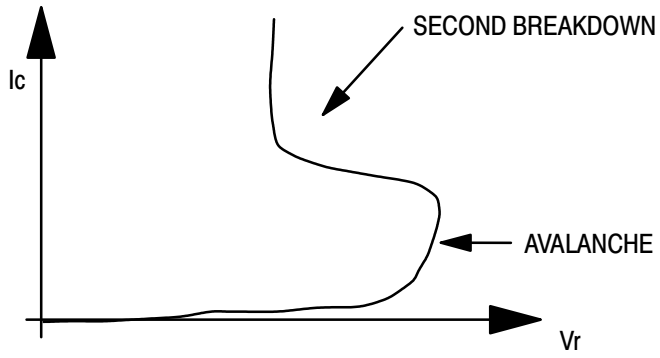


Figure 4. Typical Second Breakdown Characteristic

The initialization of this mechanism is essentially caused by the temperature effect. After a time delay following the power pulse P = Ic*BVCEO applied to the transistor, the device goes into the second avalanche area. During the time elapsed from avalanche to second breakdown, the junction is unstable and may be rapidly downgraded. In particular, the resistance of the breakdown spot becomes extremely low. During the third part of the curve, when the voltage is significantly reduced, the chip is at high temperature and the semiconductor is in the intrinsic mode near the breakdown spot location. If the current keeps increasing, the silicon melts and the transistor is permanently destroyed.

BASIC POWER TRANSISTOR GEOMETRY

The simplified cross section of a power transistor given in Figure 5 illustrates the main areas involved in the

breakdown process. When the voltage rises across the transistor, the electrical field is sustained by the N−epitaxy, the depletion region increasing accordingly. One must point out that, in reality, a modern transistor is not built with a single junction as depicted in Figure 5, but with several emitter stripes diffused into the base P−. Such technology is mandatory to get the expected static and dynamic characteristics requested in today's applications: the photo given in Figure 6 illustrates this concept.

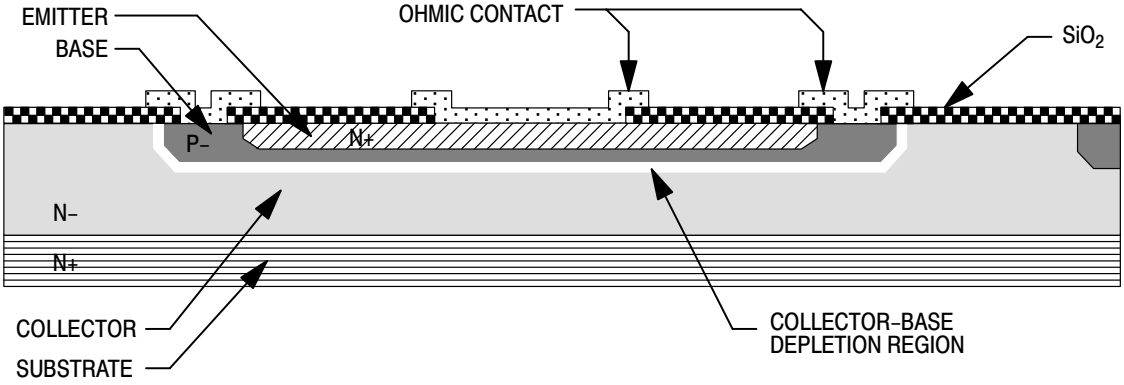


Figure 5. Simplified Cross Section of a Bipolar Power Transistor

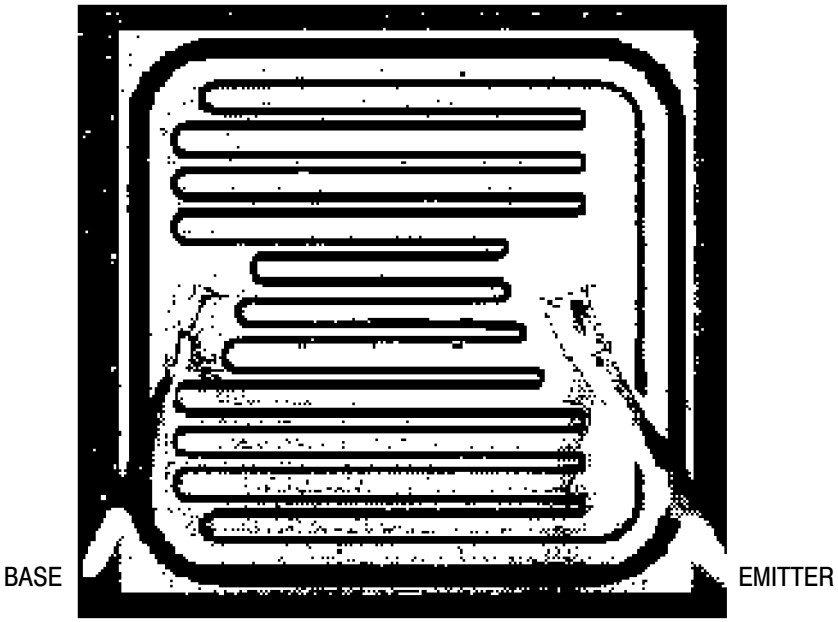


Figure 6. Photo of a Typical Power Transistor Using the PLANAR Termination

On top of that, the electrical field must not collapse at the edge of the chip, where the base diffusion no longer exists. To prevent this mode of failure, the transistors are designed with a junction termination suited for the kind of device under development. A junction termination example is given in Figure 7

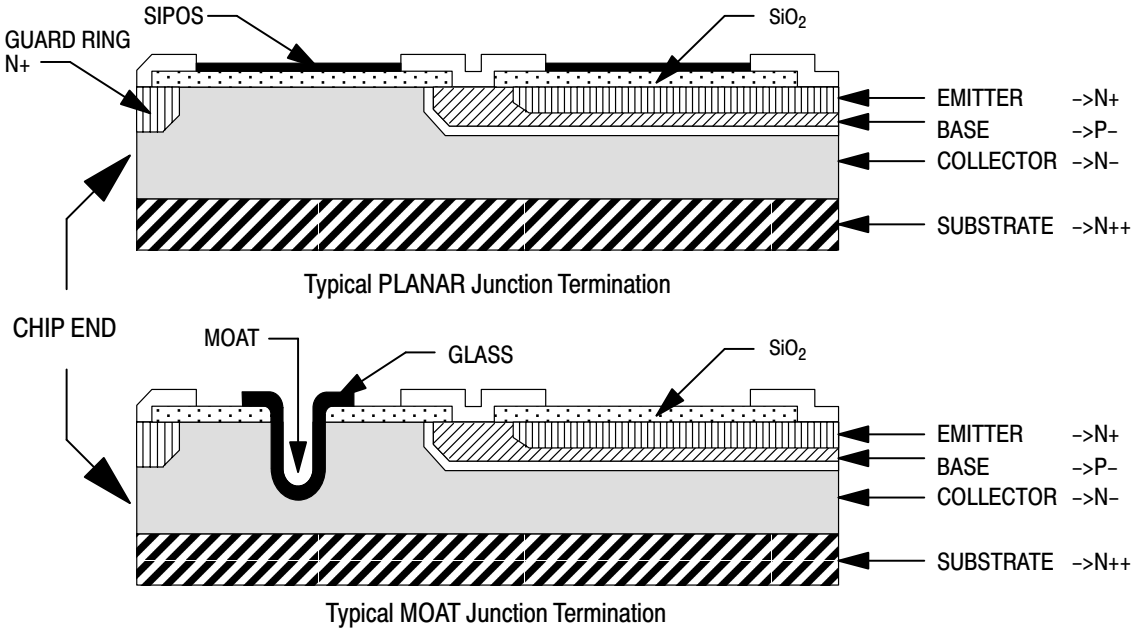


Figure 7. Typical Junction Terminations for a High Voltage Bipolar Transistor

At the time of printing this document, the PLANAR process is the most widely used technology to manufacture power transistors. However, the MOAT termination is still used for very high voltage device with BVCBO of 1500 V and above.

DYNAMIC BREAKDOWN CHARACTERISTICS

Although the static breakdown characteristics are valuable to define the performances of a semiconductor device, they do not provide all the informations needed to safely use a power transistor. Leaving aside the switching parameters, the dynamic behaviour of a power transistor is bounded by three main parameters:

FBSOA: Forward Bias Safe Operating Area

RBSOA: Reverse Bias Safe Operating Area

BVsus: Breakdown Sustaining

The designer of a given application must carefully check that, under no circumstances, the transistor will operate out of the curves provided in the data sheet: severe damage, or destruction, occurs if the operating point moves outside the specified limits.

FBSOA

The FBSOA curves are specified to define the maximum safe operating area for a given device. This parameter depends on the chip geometry and the process used to built the transistor. Particularly, the emitter fingers perimeter is extremely important since it highly influences the current spread across the silicon. As a matter of fact, at turn on, the current starts to flow from the periphery of the emitter finger, as depicted in Figure 8 The rbb' increases as we move toward the center of the emitter finger and the Base−Emitter junction is not fully forward biased during the first microseconds. Consequently, the current density is maximum at the edge of the junction and the emitter becomes prone to local hot spots.

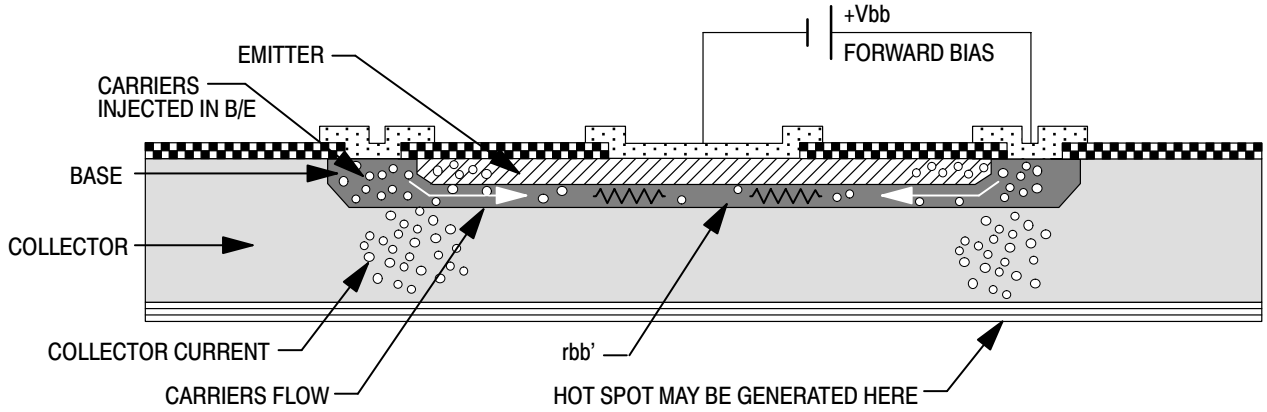


Figure 8. Turn on Mechanism for a Bipolar Power Transistor

The data provided for the FBSOA curve are based on a maximum junction temperature of +150°C and is bounded by four points as shown in Figure 9:

BVCEO: maximum allowable voltage
Icm: maximum allowable collector current
Second breakdown
Pm: maximum power dissipation
Pw: pulse width

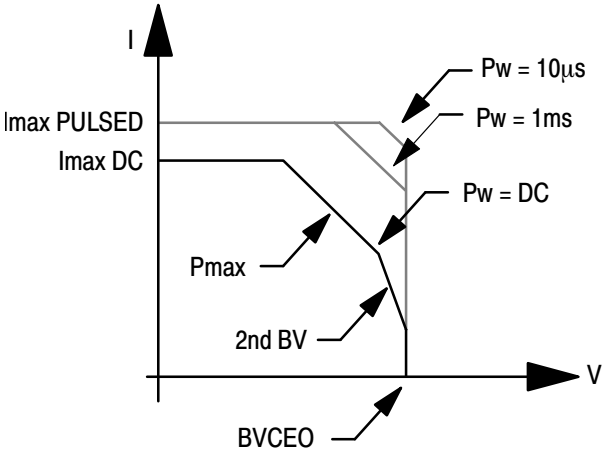


Figure 9. Typical FBSOA Curve

Since this parameter is temperature dependant, for a constant power, the FBSOA depends upon the pulse width. When the pulse is very short, below 1μs, the curves can be extended above the BVCEO limit for transistors specifically designed for switching applications.

The typical FBSOA test circuit is given in Figure 10 Cares must be observed to avoid overheating the silicon during the test. Of particular importance are the short pulses which have a high energy content since such pulses can generate a local hot spot within the silicon chip, even though the case temperature stays at ambient temperature.

Since the FBSOA test can damage the transistor, one must not re−use devices exposed to a characterization procedure. On the other hand, using conventional power supplies to bias the device under test is not recommended since they do not have the capability to accurately control either the pulse width or the current amplitude. It is preferable to use commercial equipment designed for that purpose, or to built a specific test jig, with appropriate dynamic performances, to evaluate a limited number of devices.

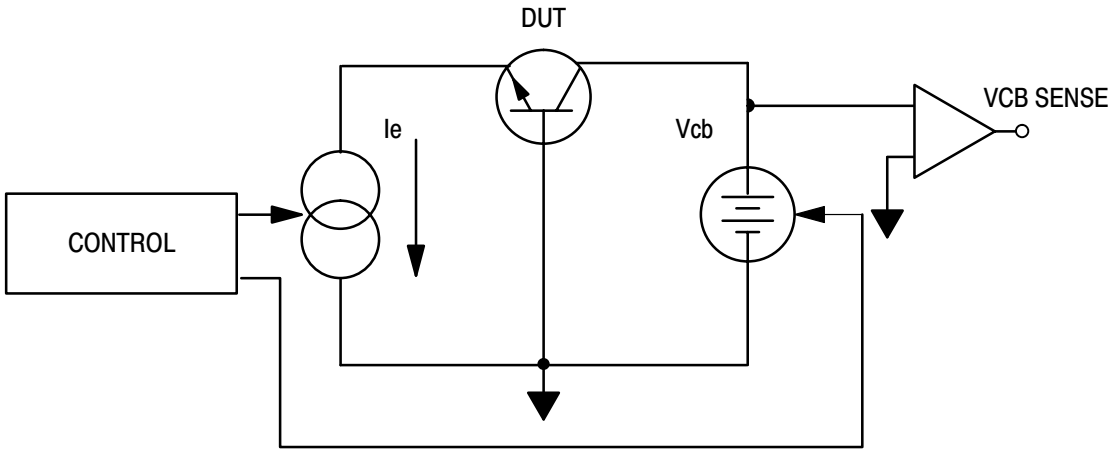


Figure 10. Typical Forward Bias Safe Operating Area Test Circuit

RBSOA

The RBSOA curves are used to define the maximum current/voltage a transistor can sustain under Base−Emitter reverse bias. As depicted by the typical test circuit given in Figure 11, this parameter is essentially an analysis of the breakdown, under dynamic condition, when the device is loaded by an inductor.

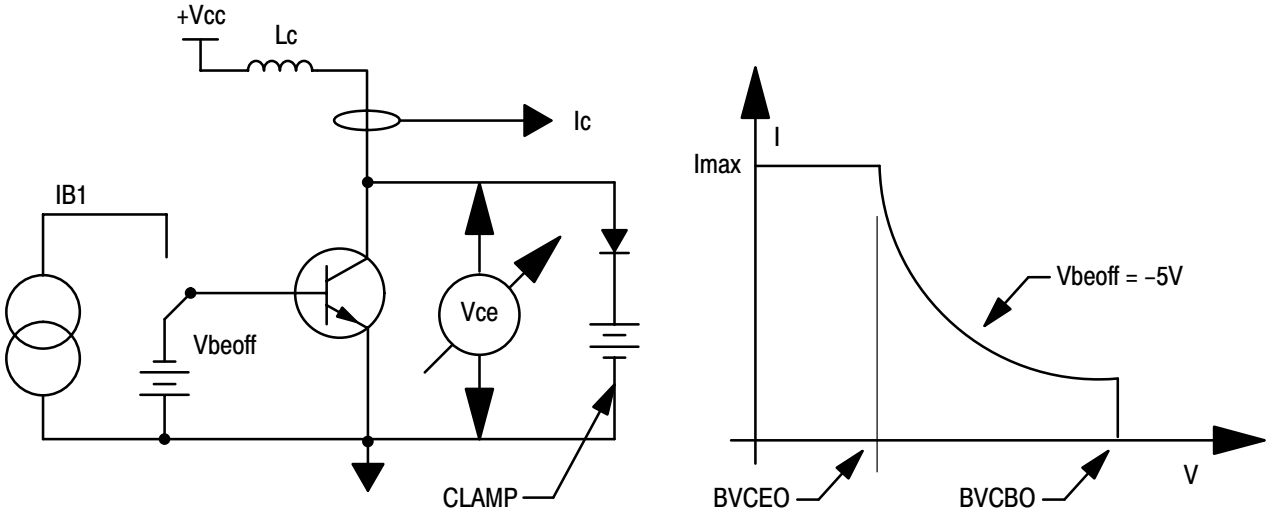


Figure 11. Typical Reverse Bias Safe Operating Area Test Circuit

The test is normally performed with a clamp connected across emitter−collector to limit the voltage within the BVCES/BVCEX of the device under test. In this case, the transistor is not avalanched and most of the energy stored into the inductor is dissipated in the clamp circuit. As a matter of fact, when a voltage clamp is used, the transistor sustains the current−voltage stress only during its collector current fall time.

The same parameter can be evaluated without providing a voltage clamp: in this case, the transistor will be forced in the avalanche region (assuming L*(dI/dt) > BVCES) and all the energy accumulated in the inductor will be dissipated into the device under test. This condition forces much more stress into the silicon as the current will flow during a longer time than the collector current fall time (all of the $1/2L*I^2$ energy must be dissipated) under avalanche condition. Extreme care must be observed when performing such a test since the transistor is very rapidly destroyed if the current is not carefully limited by the external circuit. As a standard rule, the test is carried out by slowly increasing the voltage clamp until the transistor goes into avalanche, the current being limited by the pulse width applied during the charging time of the inductor.

The RBSOA test is sometime named sustaining breakdown (BVCEsus) when it is performed unclamped, or inductive switching when the collector voltage is clamped below BVCES.

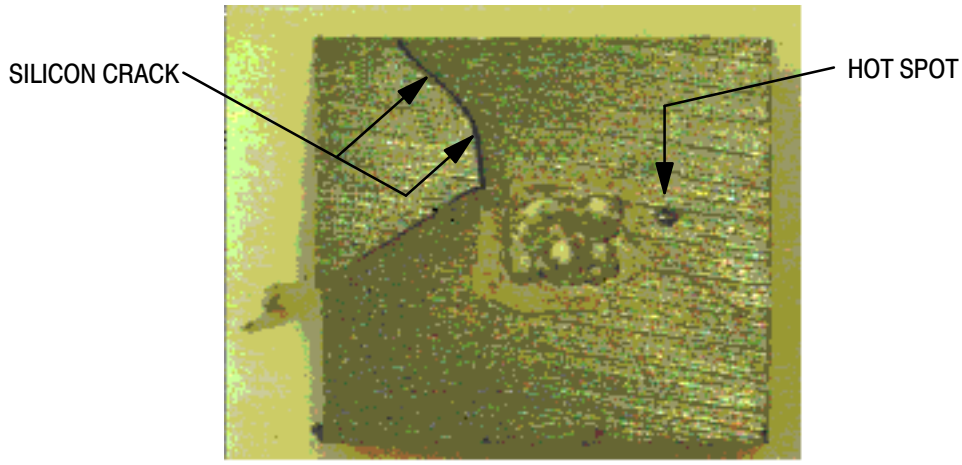


Figure 12. (a) Microphotography of a Power Transistor Damaged by a RBSOA

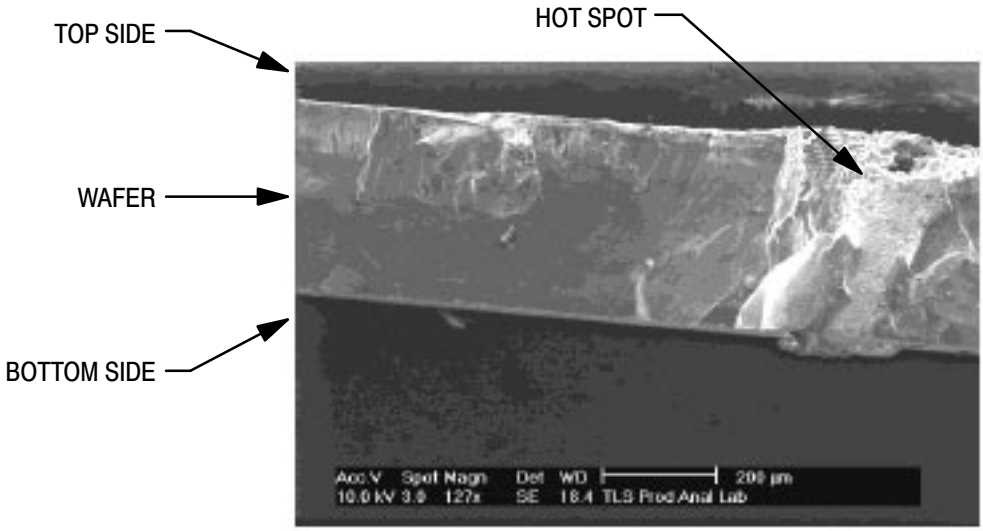


Figure 12.(b) Cross Section of the Damaged Chip (given Fig. 12a) Showing how the Silicon Melts.

POWER DEVICE BEHAVIOUR

The reverse bias characteristics of a power transistor are split into two families: the leakage current and the breakdown.

Generally speaking, the leakage current tests do not generate high stress into the chip, unless the transistor under test has a voltage capability well below the voltage bias. As a matter of fact, since the bias voltage is defined prior being forced across the junction, there is no snap back in the characteristic and the test circuit remains stable. On top of that, leakage currents are in the micro ampere range, for modern silicon power transistors, and the power generated during the test cannot damage the chip. As an example, let us assume an ICEO test performed at 400 V, the maximum current being 100 μA, yielding 40mW in the junction. This value is well within the power handling capability of the transistor and cannot damage the device.

However, although they provide reliable informations, the leakage tests characterize neither the breakdown voltage nor the avalanche mode of a bipolar transistor. These behaviour are analyzed by means of the safe operating area tests as discussed above.

When the transistor is tested in BVCEO, the current/voltage characteristic exhibit a snap back effect when the Collector/Emitter voltage jumps from the breakdown to the test point point defined at a higher current. This phenomenon, illustrated in Figure 13, is prone to heavy uncontrolled oscillation due to the negative impedance which is developed from point A to point B.

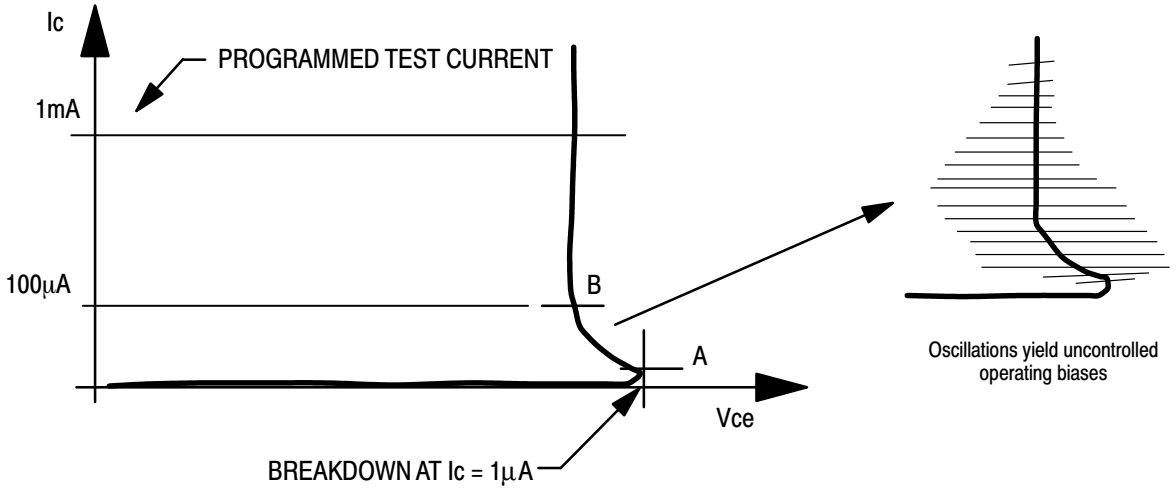


Figure 13. Typical BVCEO Characteristic

Such behaviour can be observed with a curve tracer by limiting the power dissipated into the transistor.

The power transistors are characterized, among others parameters, by a set of breakdown curves as depicted in Figure 14 Under no condition can the transistor be exposed to a voltage−current above the maximum rating provided in the data sheets.

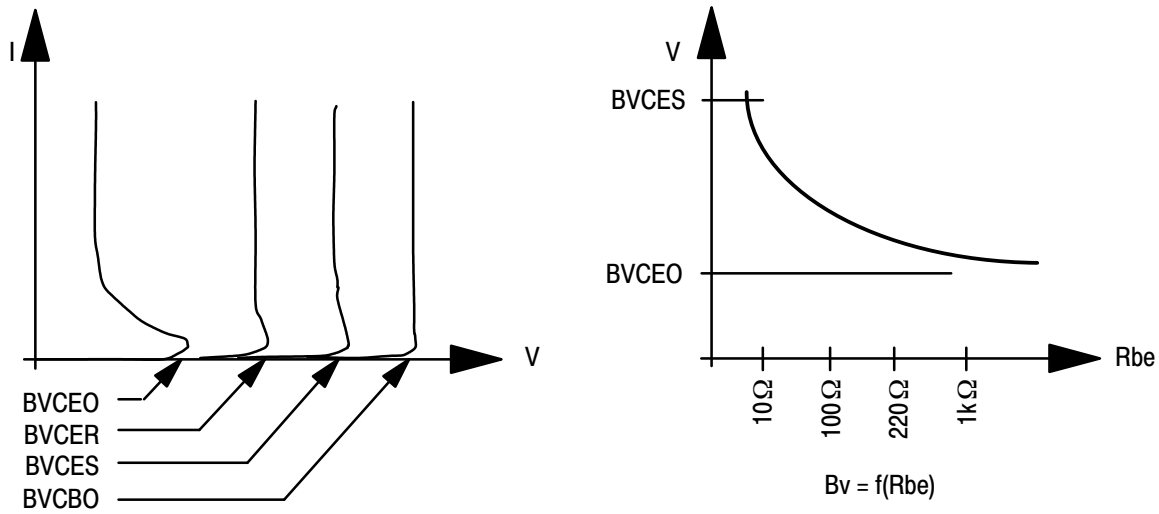
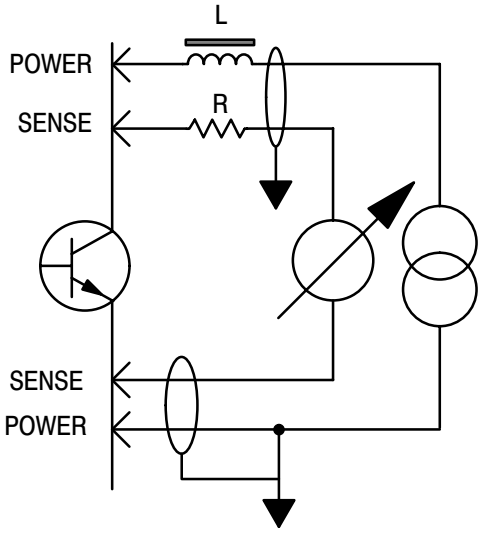
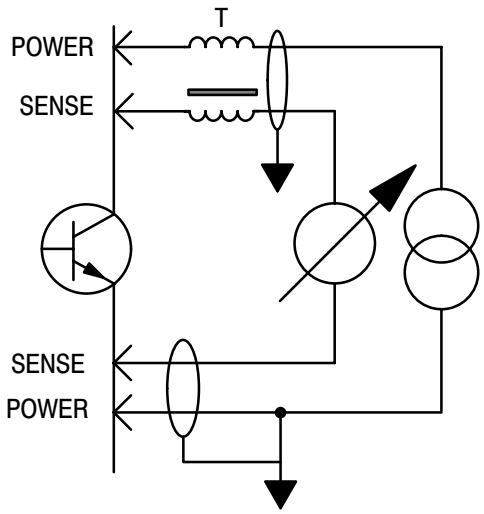


Figure 14. Typical Breakdown Curves (BVEBO not shown)

Because the current source used to perform the breakdown test has a high voltage compliance (in fact, the open load voltage must be higher than the maximum breakdown voltage one expects to characterize), it is not easy to make it oscillation free when the load is very variable. The problem can be cured by using anti oscillation networks right across the transistor electrodes (see Figure 15), but the device can be damaged or destroyed if the current rises above the maximum value allowable for a given chip.



The values of R and L are adjusted for a given transistor and test conditions. Typical values are R=470 Ω and L=100 μH. All the network must be located as close as possible to the transistor under test.
Kelvin contacts are mandatory. Shielding cables are recommended.

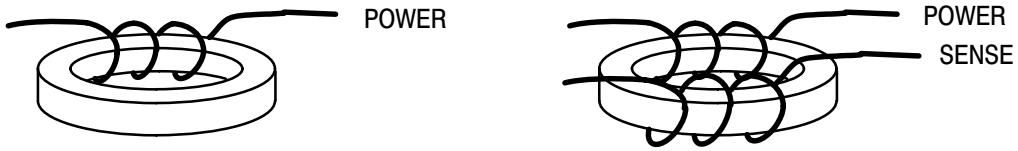


The transformer T1 provides an AC feedback to the current source and is adjusted for a given set of test conditions.
Typically, the primary inductance is 100 μH with Np/Ns=1.

Figure 15. Typical Anti Oscillation Networks

It is also possible to use a capacitor, connected across Collector−Base of the transistor under test, to generate a local AC feedback, although this is not recommended. Keeping in mind that the current source associated with the transistor is a high gain transconductance amplifier, any LC network connected across it generates high frequency oscillations that will make the BVCEO test impossible. Since one cannot define accurately the parasitic inductances and stray capacitances existing in the test circuit, it is preferable not to use a capacitive feedback across the transistor.

The inductor L and the transformer T can be built around a toroid using a high permeability ferrite material. A typical application is given in Figure 16



Toroid: 16x20
Ferrite: N27, B50, A4A
The transformer may require a larger core to accommodate the primary and secondary turns. Using a high permeability material limits the number of turns needed to get the expected inductance.

Figure 16. Typical Inductor Design

One must point out that the design of such an anti−oscillation network very much depends on the test system used to measure the breakdown. Consequently, it's not easy to modelize an accurate circuit and several attempts are usually necessary to tune the network for a given environment.

Another issue with the BVCEO test is the discharge of stray capacitances into the transistor. When the tests are carried out with an automatic instrument, the cables can be several meter in length and the stray capacitance becomes non negligible and are charged up to BVCEO when the current source is connected to the device. Since this source has a finite settling time (i.e., the current does not stabilize to the programmed value in less than a few tens of microseconds!), the current coming from the discharge of the stray capacitance cannot be controlled and may damage the chip within a few micro second. This is particularly true for the BVCEO test as depicted in Figure 17: during the negative going slope, the Collector/Emitter voltage collapses, discharging the

stray capacitance by the delta V from A to B, yielding a peak current above the programmed value.

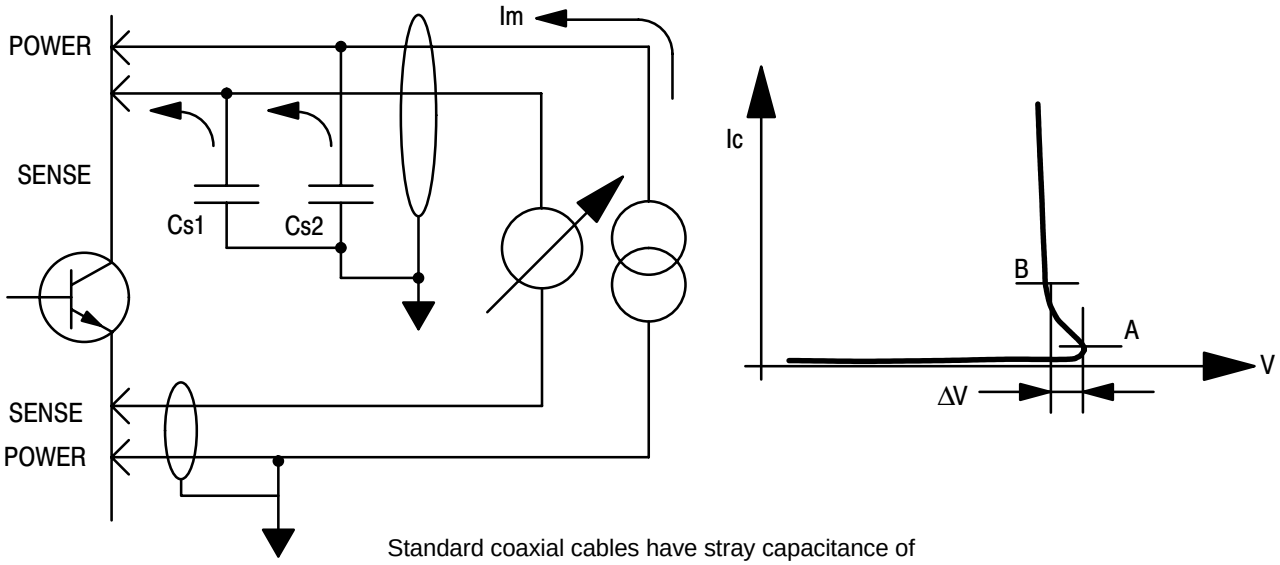


Figure 17. Stray Capacitances Effect

Assuming a Δ V of 60 V and a total series resistance of 10 Ω, the peak current flowing from the stray capacitances Cs1/Cs2 as depicted in Figure 16, is 6 A. On the other hand, most of the automatic test handler are connected to the tester by coaxial cables up to five meters long. In this case, the total stray capacitance (combining Power and Sense) is 1000 pF, yielding a time constant of:

$Pw = 5*\Sigma Cs*\Sigma R$

$Pw = 5*1000*10^{-12}*10$

$Pw = 50ns$

During this amount of time, the transistor must dissipate the energy accumulated in Cs1 & Cs2:

$Ej = \Sigma Cs*\Delta V^2*0.5$

$Ej = 1000*10^{-12}*60*60*0.5$

$Ej = 1.8\mu J$

This value cannot damage the transistor but, if the circuit oscillates, the Δ V can be much higher and, for a high voltage power transistor, the energy can rise to a value above the maximum capability of the junction. As an example, let us assume Δ V = 500 V, then Ej = 125 μJ. Of course, a power transistor can easily handle such amount of energy, but the same transistor can be rapidly damaged when the energy is generated during the transient phase of the breakdown mechanism. As a matter of fact, during uncontrolled oscillation, most of the energy developed in the circuit will be dissipated in a very small area of the die, yielding a very high current density which, in turn, generates a hot spot in the silicon. Ultimately, the silicon may melt and the device is destroyed. This is a consequence of the multiplication factor **M** as discussed above.

Consequently, it's recommended to reserve the breakdown test for engineering and characterization purpose, using the leakage current test to perform, incoming inspection. However, the breakdown parameters are fully tested, under several biases and case temperatures, during the development of a new power transistor. Regular samplings also provide statistics, at production level, to make sure the devices are fully within the guaranteed limits published in the data sheet.

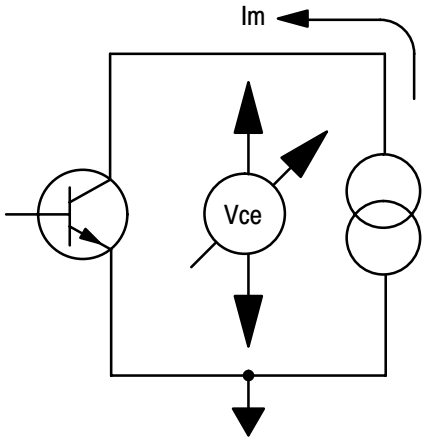
PARAMETERS DEFINITIONS

The off condition parameters are split into two families: the leakage currents and the breakdown voltages. Both are characterized during the development of a transistor and tested during the final test process. The voltage spans from a low 6.00 V for the Bvebo, to a high 1800 V for the Bvcbo, the leakage currents ranging from nano ampere to one milli ampere at room temperature.

BREAKDOWN VOLTAGES

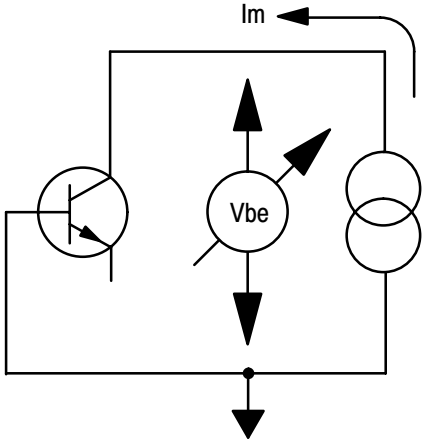
BVCEO: reverse Collector to Emitter voltage, with the Base open, under a given collector current bias.

Im: programmed
Vce: measured



BVCBO: reverse Collector to Base voltage, with the Emitter open, under a given collector current bias.

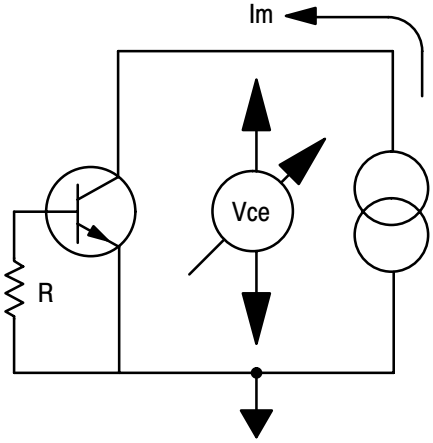
Im: programmed
Vcb: measured



BVCER: reverse Collector to Emitter voltage, the Base connected to the Emitter with a low ohm resistor, under a given Collector current bias.

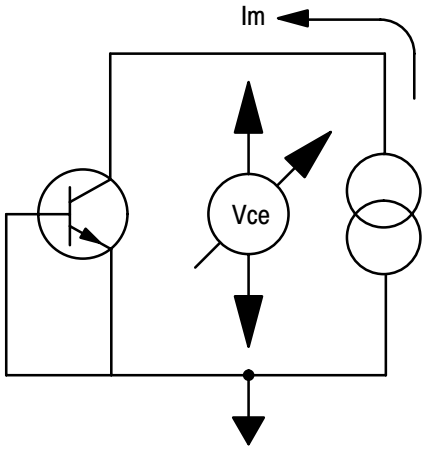
Im: programmed
Vce: measured

Resistor R must be located as close as possible of the device under test.



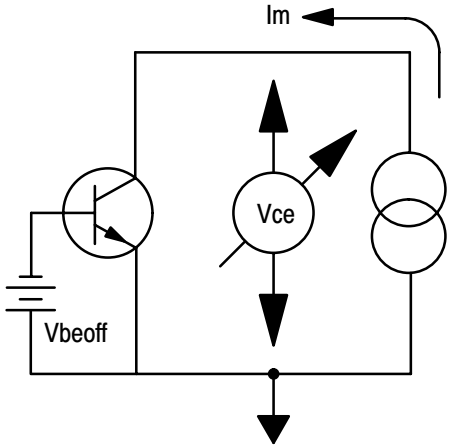
BVCES: reverse Collector to Emitter voltage, the Base shorted to the Emitter, under a given Collector current bias.

Im: programmed
Vce: measured



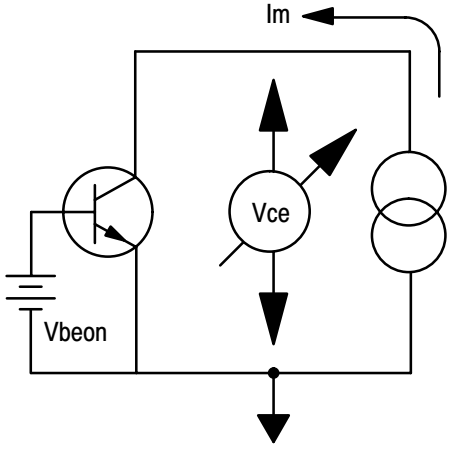
BVCEX: reverse Collector to Emitter voltage, with a reverse Base to Emitter bias, under a given Collector current bias.

Im: programmed
Vce: measured



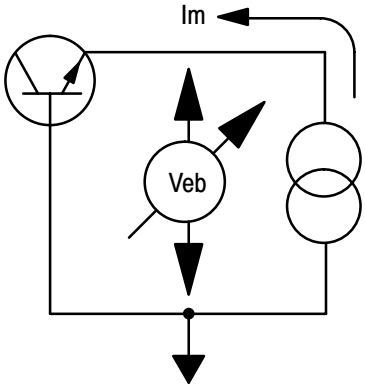
BVCEY: reverse Collector to Emitter voltage, with a forward Base to Emitter bias, under a given Collector current bias.

Im: programmed
Vce: measured



BVEBO: reverse Emitter to Base voltage, with the Collector open, under a given Emitter current bias.

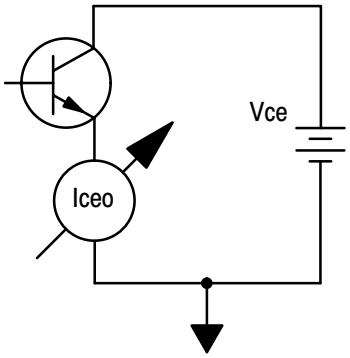
Im: programmed
Vce: measured



LEAKAGE CURRENTS

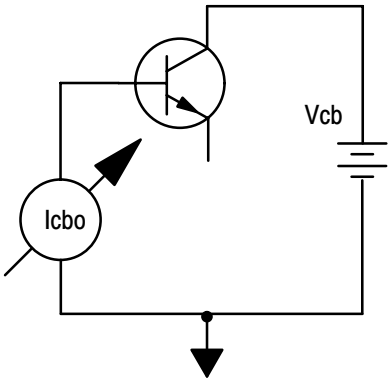
ICEO: Collector to Emitter current under reverse Collector to Emitter voltage, Base open.

Vce: programmed
Iceo: measured



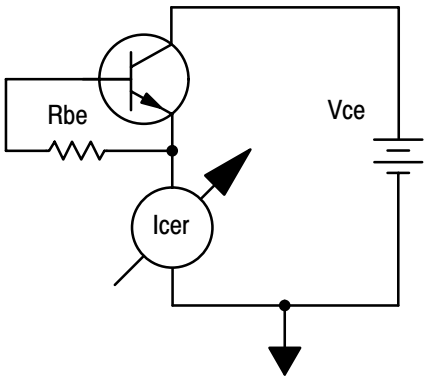
ICBO: Collector to Base current under reverse Collector to Base voltage, Emitter open.

Vcb: programmed
Icbo: measured



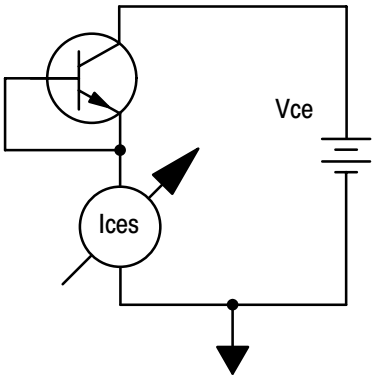
ICER: Collector to Emitter current under reverse Collector to Emitter voltage, Base connected to Emitter by a low ohm resistor.

Vce: programmed
Icer : measured.



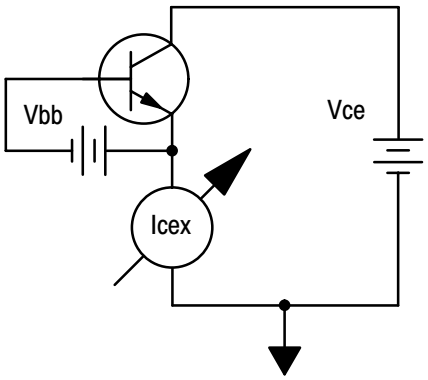
ICES: Collector to Emitter current under reverse Collector to Emitter voltage, Base shorted to Emitter.

Vce: programmed
Ices: measured



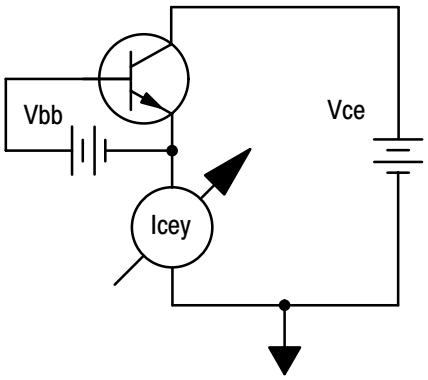
ICEX: Collector to Emitter current under reverse Collector to Emitter voltage, with a reverse Base to Emitter bias.

Vce: programmed
Icex: measured



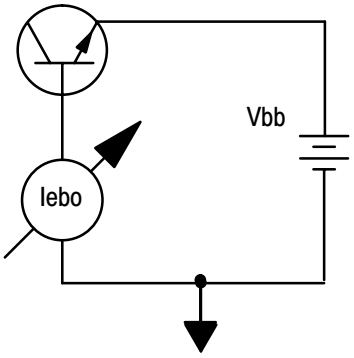
ICEY: Collector to Emitter current under reverse Collector to Emitter voltage, with a forward Base to Emitter bias.

Vce: programmed
Icey: measured



IEBO: Emitter to Base current under reverse Emitter to Base voltage, Collector open.

Vbb: programmed
Iebo: measured



ANNEXES

Symbols

E:	Electrical field
E_1:	minimum energy for ionizing collision
E_g:	Band Gap energy
q:	electron charge
n:	electron density
np:	excess electron density (p region)
L:	mean free path
M:	avalanche multiplication factor
α_n:	ionization coefficient for electrons
α_p:	ionization coefficient for holes

Breakdown Electrical Fields in Semiconductors

Material	Bandgap (eV)	Breakdown Electrical Field (V/cm)
GaAs	1.43	$4*10^5$
Ge	0.664	10^5
InP	1.34	–
Si	1.10	$3*10^5$
$In_{0.53}Ga_{0.47}As$	0.80	$2*10^5$
C	5.50	10^7
SiC	2.9	$2.5*10^6$
SiO_2	9	10^7
Si_3N_4	5	10^7

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